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09/277,893	03/29/1999	KENNETH W. MARR	3543US(97-95	4223

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/277,893	MARR	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-33,50-72 and 74-101* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-33,50-72 and 74-101* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17, 19-24, 26-33, 102 and 103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. in view of Chen (USPAT 5712206).

Fischer et al. discloses a method of fabricating a fuse upon a semiconductor device in figures 1 – 3.

With regard to claim 17, in figure 1 Fischer et al. discloses disposing a layer of conductive material (11) over an insulative structure (10) of the semiconductor device. Fischer also discloses in figure 1 patterning the layer of conductive material to define at least two spaced apart terminal sites. Fischer et al. also discloses in figure 3 removing conductive material of the layer in areas around the spaced apart terminal sites. Fischer et al. discloses in figure 2 disposing a second conductive layer (12) over the semiconductor device, including adjacent to the insulative structure exposed between the at least two terminal sites. In figure 3 Fischer et al. discloses patterning the second conductive layer so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two terminal sites of conductive material, and a central region disposed between the at least two terminal regions and in

contact with the insulative structure. Fischer et al. does not disclose the second conductive layer as a metal silicide. Chen teaches in column 5, lines 57 – 65 a conductive layer (62) for a fuse that is a metal silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the metal silicide layer of Chen in the method of fabricating a fuse upon a semiconductor device of Fischer et al. in order to use a preferred conductive material for the fuse that is well known in the art as stated by Chen in column 5, lines 57 – 65.

With regard to claims 19, the method of Fischer et al. discloses in column 3, lines 42 - 50 patterning the layer of conductive material comprising disposing a mask over the semiconductor device and removing selected regions of the layer of conductive material through the mask.

With regard to claim 20, Fischer et al. does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto the semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al. in order to pattern the metal layer.

With regard to claims 21 and 22, the method of Fischer et al. discloses in column 3, lines 34 – 50 that the removing comprises isotropically etching the selected regions of the layer of conductive material through the mask.

With regard to claim 23, Fischer et al. does not disclose etching the selected regions of the layer of conductive material with a wet etch. It is well known in the art

that etching can comprise wet etching the selected regions of the layer of conductive material. It would have been obvious to one of ordinary skill in the art to use the wet etching method in the process of Fischer et al. in order to etch the conductive material with tapered edges.

With regard to claim 24, Fischer et al. discloses in column 2, lines 45 – 48 disposing the layer of conductive material comprises chemical vapor depositing the layer of conductive material.

With regard to 26, Chen discloses in column 5, lines 57 – 65 the metal silicide is tungsten silicide.

With regard to claim 27, the method of Fischer et al. and Chen inherently disclose patterning the layer of metal silicide comprising disposing a mask over the semiconductor device and removing selected regions of the layer of metal silicide through the mask.

With regard to claim 28, Fischer et al. and Chen do not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto the semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al. and Chen in order to pattern the metal silicide.

With regard to claims 29 and 30, the method of Fischer et al. and Chen inherently disclose that the removing comprises anisotropically etching the selected regions of the layer of metal silicide.

With regard to claim 31, Fischer et al. does not disclose etching the selected regions of the layer of the metal silicide with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions of the layer of metal silicide. It would have been obvious to one of ordinary skill in the art to use the dry etching method in the process of Fischer et al. and Chen in order to etch the metal silicide with vertical edges.

With regard to claim 32, it is inherent that a contact is disposed in communication with at least one of the at least two terminal regions.

With regard to claim 33, it is inherent that another contact is disposed in communication with another of the at least two terminal regions.

With regard to claim 102, in Fischer et al. figure 3 the removing comprises exposing the insulating structure 10 around the terminal sites.

With regard to claim 103, the removing comprises exposing the insulating structure beneath the areas.

3. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. and Chen as applied to claim 17 above, and further in view of Mitani (JPPAT 59-154038).

With regard to claim 18, Fischer et al. and Chen do not disclose that disposing the layer of the conductive material comprises disposing polysilicon onto the insulative structure. Mitani discloses in figures 1 and 2 disposing polysilicon (5) as a conductive material for a fuse structure (3). It would have been obvious to one of ordinary skill in

the art at the time of the present invention to dispose the polysilicon of Mitani in the method of Fischer et al. and Chen in order to dispose a conductive material layer that will be both part of the fuse component and a gate electrode as stated by Mitani in the abstract and constitution.

4. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. and Chen as applied to claim 17 above, and further in view of Sandhu.

With regard to claim 26, Fischer et al. and Chen do not disclose that the layer of metal silicide is deposited by chemical vapor deposition. Sandhu discloses in figure 1 that depositing the layer of metal silicide (12) comprises chemical vapor depositing the layer of metal silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the chemical vapor deposition process of Sandhu in the method of Fischer et al. and Chen in order to deposit a metal silicide film characterized by low impurities, good step coverage, and low stress with the silicon substrate as taught by Sandhu in the abstract.

5. Claims 50, 51, 55-60 and 62-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. in view of Mitani and Chen.

With regard to claim 50, Fischer et al. discloses in figures 1 – 3 a method of fabricating a fuse. Fischer et al. discloses in figure 1 fabricating spaced (111) apart terminal sites comprising a first conductive layer (11) on an insulative structure (10) of a semiconductor device, the insulative structure being exposed between the terminal

sites. Fischer et al. discloses in figures 2 and 3 fabricating a fuse comprising a second conductive layer (12), including a central region disposed adjacent the insulative structure and between the spaced apart terminal sites and at least two terminal regions disposed on opposite ends of the central region and adjacent the space apart terminal sites. Fischer et al. does not disclose that the first conductive layer comprises polysilicon on the insulative structure. Mitani discloses in figures 1 and 2 polysilicon (5) as a conductive layer for a fuse structure (3). It would have been obvious to one of ordinary skill in the art at the time of the present invention to dispose the polysilicon of Mitani in the method of Fischer et al. in order to use a first conductive layer that will be both part of the fuse component and a gate electrode as stated by Mitani in the abstract and constitution. Fischer et al. and Mitani do not disclose the fusible second conductive layer is a metal silicide. Chen teaches in column 5, lines 57 – 65 a fusible conductive layer (62) that is a metal silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the metal silicide layer of Chen in the method of fabricating a fuse upon a semiconductor device of Fischer et al. and Mitani in order to use a preferred conductive material for the fuse that is well known in the art as stated by Chen in column 5, lines 57 – 65.

With regard to claim 51, Fischer et al. discloses in figure 1 disposing the first conductive layer onto the insulative structure, and patterning the conductive material. As applied above the first conductive layer is polysilicon.

With regard to claims 55, the method of Fischer et al. discloses in column 3, lines 42 – 50 patterning comprises disposing a mask adjacent the first conductive layer and

removing selected regions of the conductive layer through the mask. As applied above the first conductive layer is polysilicon.

With regard to claim 56, Fischer et al., Mitani and Chen do not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist adjacent the first conductive layer, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al., Mitani and Chen in order to pattern the first conductive layer. As applied above the first conductive layer is polysilicon.

With regard to claims 57 and 58, the method of Fischer et al. discloses in column 3, lines 34 – 50 that the removing comprises isotropically etching the selected regions of the first conductive layer through the mask. As applied above the first conductive layer is polysilicon.

With regard to claim 59, Fischer et al., Mitani and Chen do not disclose etching the selected regions of the first conductive layer with a wet etch. It is well known in the art that etching can comprise wet etching the selected regions first conductive layer. It would have been obvious to one of ordinary skill in the art to use the wet etching method in the process of Fischer et al., Mitani and Chen in order to etch the first conductive layer with tapered edges. As applied above the first conductive layer is polysilicon.

With regard to claim 60, Fischer et al. discloses in figure 2 disposing the second conductive layer adjacent the spaced apart terminal sites and the insulative structure

exposed therebetween. As applied above the second conductive layer is a metal silicide.

With regard to claim 62, Fischer et al. discloses in figure 2 patterning the second conductive layer. As applied above the second conductive layer is a metal silicide.

With regard to claim 63, the method of Fischer et al., Mitani and Chen inherently discloses patterning the layer of metal silicide comprising disposing a mask over the semiconductor device and removing selected regions of the layer of metal silicide through the mask.

With regard to claim 64, Fischer et al., Mitani and Chen do not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto the semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Fischer et al., Mitani and Chen in order to pattern the metal silicide.

With regard to claims 65 and 66, the method of Fischer et al., Mitani and Chen inherently discloses that the removing comprises anisotropically etching the selected regions of the metal silicide.

With regard to claim 67, Fischer et al., Mitani and Chen does not disclose etching the selected regions of the layer of the second conductive layer with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions of the layer of second conductive layer. It would have been obvious to one of ordinary skill in

the art to use the dry etching method in the process of Fischer et al., Szluk et al. and Sandhu in order to etch the metal silicide with vertical edges.

With regard to claim 68, Fischer et al. discloses in figures 2 and 3 the patterning of the second conductive layer comprises defining the at least two terminal regions of the fuse adjacent the spaced apart regions and the central region of the fuse adjacent the insulative structure. As applied above the second conductive layer is metal silicide.

6. Claims 52 – 54, 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al., Mitani and Chen as applied to claims 50 and 51 above, and further in view of Degelormo et al.

Fischer et al., Mitani and Chen do not disclose disposing the polysilicon by chemical vapor deposition. Degelormo et al. teaches in column 6, lines 60-63 of chemical vapor depositing doped polysilicon wherein doping occurs substantially simultaneously with the disposing. The method of Degelormo et al. would further allow the spaced apart regions of polysilicon to be doped, and the doping to occur substantially simultaneously with disposing polysilicon on the insulative structure. It would have been obvious to use the polysilicon disposing method of Degelormo et al. in the method of Fischer et al., Mitani and Chen in order to make lower resistance polysilicon as stated by Degelormo et al. in column 6, lines 32 – 35.

7. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al., Mitani and Chen as applied to claims 50 and 60 above, and further in view of Sandhu.

With regard to claim 26, Fischer et al., Mitani and Chen do not disclose that the layer of metal silicide is deposited by chemical vapor deposition. Sandhu discloses in figure 1 that depositing the layer of metal silicide (12) comprises chemical vapor depositing the layer of metal silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the chemical vapor deposition process of Sandhu in the method of Fischer et al., Mitani and Chen in order to deposit a metal silicide film characterized by low impurities, good step coverage, and low stress with the silicon substrate as taught by Sandhu in the abstract.

8. Claims 71, 74-86, 88-96, 101, 104 and 105 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani in view of Fischer et al. and Chen

With regard to claim 71, and 74, Mitani discloses in figures 1 and 2 a method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate. Mitani discloses in figures 1 and 2 disposes a layer of insulative material (4) over at least an exposed region of the semiconductor substrate (1). Mitani discloses in figures 1 and 2 also disposes a layer of polysilicon (5) over the semiconductor substrate, including over the layer of insulative material and over isolation regions (2) disposed on the semiconductor substrate. Mitani discloses in figures 1 and 2 patterning at least regions of the layer of polysilicon (5) disposed over at least one isolation region of the

isolation regions. Mitani discloses in figures 1 and 2 forming a layer of metal silicide (6) on the layer of polysilicon. Mitani does not disclose defining at least two spaced apart terminal sites of polysilicon. Fischer et al. teaches in figure 1 patterning regions (11) comprising defining at least two spaced apart terminal sites of a conductor layer on at least one isolation region (10) and between which a portion of the at least one isolation region is exposed therebetween. Fischer et al. also teaches in figure 2 and 3 defining a fuse comprising defining a central region (111) disposed adjacent and substantially between the at least two spaced apart terminal sites and defining at least two terminal regions, each terminal region continuos with an end of the central region and disposed adjacent one of the at least two spaced apart terminal sites. Fischer also teaches in figure 3 removing conductive material of the layer from areas of the layer located around the at least two spaced apart terminal sites. It would have been obvious to one of ordinary skill in the art at the time of the present invention to pattern the silicon layer of Mitani with the two spaced apart terminal sites of Fischer et al. in order to create a laser-programmable or electric-current-programmable link features having locally reduced cross-sectional area resulting from locally reduced thickness of a conductive path, while width remains essentially constant, as stated by Fischer et al. in column 1, lines 60 – 65. Mitani and Fischer et al. do not disclose the fusible second conductive layer is a metal silicide. Chen teaches in column 5, lines 57 – 65 a fusible conductive layer (62) that is a metal silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the metal silicide layer of Chen in the method of fabricating a fuse upon a semiconductor device of Mitani and Fischer et al. in

order to use a preferred conductive material for the fuse that is well known in the art as stated by Chen in column 5, lines 57 – 65.

With regard to claim 75, the method of Mitani, Fischer et al. and Chen defining the at least two spaced apart terminal sites inherently comprises disposing a mask over the layer of polysilicon and removing selected regions of the layer of polysilicon through the mask.

With regard to claim 76, Mitani, Fischer et al. and Chen do not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask over a layer of polysilicon, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Mitani, Fischer et al. and Chen in order to pattern the polysilicon.

With regard to claims 77 and 79, the method of Mitani, Fischer et al. and Chen inherently discloses that the removing comprises isotropically etching the polysilicon.

With regard to claim 78, Mitani, Fischer et al. and Chen do not disclose etching the selected regions with a wet etch. It is well known in the art that etching can comprise wet etching the selected regions of polysilicon. It would have been obvious to one of ordinary skill in the art to use the wet etching method in the process of Mitani, Fischer et al. and Chen in order to etch the polysilicon to have slanted sidewalls.

With regard to claims 80 and 81, Mitani discloses in figures 1 and 2 patterning gate regions of the layer of polysilicon that occurs substantially simultaneously with the patterning the at least regions of the layer of polysilicon.

With regard to claim 82, the method of Mitani inherently comprises disposing a mask over the layer of polysilicon and removing selected regions of the layer of polysilicon through the mask.

With regard to claim 83, Mitani does not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask onto a semiconductor device, expose selected regions of the photoresist and develop the selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Mitani in order to pattern the polysilicon.

With regard to claims 84 and 86, the method of Mitani inherently discloses that the removing comprises anisotropically etching the selected regions.

With regard to claim 85, Mitani does not disclose etching the selected regions with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions. It would have been obvious to one of ordinary skill in the art to use the dry etching method in the process of Mitani in order to etch the polysilicon to have vertical sidewalls.

With regard to claim 88, the method of Mitani, Fischer et al. and Chen defining the gate from at least the layer of metal silicide inherently comprises disposing a mask over the layer of metal silicide and removing selected regions of the layer of metal silicide through the mask.

With regard to claim 89, Mitani, Fischer et al. and Chen do not disclose that the mask is photoresist. It is well known in the art to dispose a photoresist mask over a layer of metal silicide, expose selected regions of the photoresist and develop the

selected regions. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the photoresist method in the method of Mitani, Fischer et al. and Chen in order to pattern the metal silicide.

With regard to claims 90 and 92, the method of Mitani, Fischer et al. and Chen inherently discloses that the removing comprises anisotropically etching the selected regions.

With regard to claim 91, Mitani, Fischer et al. and Chen do not disclose etching the selected regions with a dry etch. It is well known in the art that etching can comprise dry etching the selected regions. It would have been obvious to one of ordinary skill in the art to use the dry etching method in the process of Mitani, Fischer et al. and Chen in order to etch the metal silicide to have vertical sidewalls.

With regard to claims 93 – 96, Mitani, Fischer et al. and Chen read on the claimed invention either inherently or obviously as applied to similar above claims.

With regard to claim 101, Mitani discloses in figure 1 doping at least one source region (18) and at least one drain region (19) of the semiconductor substrate, the at least one source region and the at least one drain region disposable adjacent the gate on opposite sides thereof.

With regard to claim 104, the removing of Fischer et al. further comprises exposing the insulating structure beneath the areas.

With regard to claim 105, the removing comprises exposing an insulating structure beneath the areas.

9. Claim 72 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani, Fischer et al. and Chen as applied to claim 71 above, and further in view of Degelormo et al.

As far as the examiner can ascertain the rejections below read on the claimed invention.

Mitani, Fischer et al. and Chen do not disclose disposing the polysilicon by chemical vapor deposition. Degelormo et al. teaches in column 6, lines 60-63 of chemical vapor depositing doped polysilicon. It would have been obvious to use the polysilicon disposing method of Degelormo et al. in the method of Mitani, Fischer et al. and Chen in order to make lower resistance polysilicon as stated by Degelormo et al. in column 6, lines 32 – 35.

10. Claim 87 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani, Fischer et al. and Chen as applied to claim 71 above, and further in view of Sandhu.

As far as the examiner can ascertain the rejections below read on the claimed invention.

Mitani, Fischer et al. and Chen do not disclose disposing metal silicide by chemical vapor deposition. Sandhu teaches in figure 1 disposing a layer of metal silicide comprising chemical vapor depositing the layer of metal silicide (12). It would have been obvious at the time of the present invention to use the disposing of metal silicide method of Sandhu in the method of Mitani, Fischer et al. and Chen in order to

use the properties of low bulk resistance and low stress of the metal silicide as stated by Sandhu in column 1, lines 12 – 21.

11. Claims 97 – 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani, Fischer et al. and Chen as applied to claim 71 above, and further in view of Ukeda et al.

As far as the examiner can ascertain the rejections below read on the claimed invention.

Mitani, Fischer et al. and Chen do not disclose removing exposed regions of the insulative material through the layer of polysilicon. Ukeda et al. discloses in figures 1f and 1g and columns 3 and 4, lines 64 – 67 and 1 – 15 respectively removing exposed regions of the layer of insulative material (2) through the layer of polysilicon by anisotropically, dry etching the exposed regions of insulative material. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the removing methods of Ukeda et al. in the method of Mitani, Fischer et al. and Chen in order to complete the formation of a transistor furnished with a gate electrode as described by Ukeda et al. in column 4, lines 10 – 15.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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